Amendments to the Claims:

Please cancel claim 1, amend claims 2-8, 30 and 31 and add new claims 33-40 as shown in the listing of claims that follows.

This listing of claims will replace all prior versions and listings of claims in the application:

1. (canceled).

2. (currently amended) The system of claim [[1]] 33 wherein the ~~at least one~~ delay adjuster comprises at least one adjustable delay buffer.

3. (currently amended) The system of claim [[1]] 33 wherein the ~~at least one~~ phase comparator comprises:

a rising edge phase comparator for comparing a rising edge of the first clock signal with a rising edge of the second clock signal, for generating at least one rising edge compensation signal indicative of a phase difference between the rising edge of the first clock signal and the rising edge of the second clock signal; and

a falling edge phase comparator for comparing a falling edge of the first clock signal with a falling edge of the second clock signal, for generating at least one falling edge compensation signal indicative of a phase difference between the falling edge of the first clock signal and the falling edge of the second clock signal.

4. (currently amended) The system of claim [[1]] 33 wherein the at least one ~~adjustable~~ delay ~~buffer~~ adjuster:

delays the rising edge of the first clock signal in response to the rising edge compensation signal; and

delays the falling edge of the first clock signal in response to the falling edge compensation signal.

5. (currently amended) The system of claim 2 wherein the at least one adjustable delay buffer comprises:

at least one buffer transistor for buffering the first clock signal; and

at least one control transistor, responsive to the at least one compensation signal, for adjusting current flow through the at least one buffer transistor for controlling delay of the first clock signal through the at least one buffer transistor.

6. (currently amended) The system of claim ~~1 further comprising~~ 7 wherein the first clock tree comprises a plurality of buffers for generating the first clock signal and the second clock tree comprises a plurality of buffers for generating the second clock signal.

7. (currently amended) The system of claim [[6]] 33 wherein the ~~plurality of buffers~~ first clocking circuitry comprises a ~~plurality of~~ first clock tree[[s]] and the second clocking circuitry comprises a second clock tree.

8. (currently amended) The system of claim [[1]] 33 further comprising at least one power supply for providing the first ~~supply~~ operating voltage ~~level~~ and the second ~~supply~~ operating voltage ~~level associated with the plurality of signal levels~~.

9. (previously presented) The system of claim 1 wherein the first clock signal and the second clock signal are derived from a common clock signal.

10-29. (canceled)

30. (currently amended) A method for compensating for phase differences between a plurality of clock signals associated with a plurality of signal levels, comprising the steps of:

modifying a signal level of a ~~first~~ clock signal ~~associated with a first signal level~~ to generate a ~~second~~ first clock signal associated with a ~~second~~ first signal level that is different than ~~the first~~ a second signal level associated with a second clock signal;

comparing a phase of the first clock signal with a phase of the second clock signal to generate at least one compensation signal indicative of a phase difference between the first clock signal and the second clock signal; and

delaying the first clock signal to compensate for the phase difference between the first clock signal and the second clock signal.

31. (currently amended) The method of claim 30 wherein:

the comparing step further comprises the steps of:

comparing a rising edge of the first clock signal with a rising edge of the second clock signal to generate a rising edge compensation signal indicative of a phase difference between the rising edge of the first clock signal and the rising edge of the second clock signal; and

comparing a falling edge of the first clock signal with a falling edge of the second clock signal to generate a falling edge compensation signal indicative of a phase difference between the falling edge of the first clock signal and the falling edge of the second clock

signal;

and the delaying step further comprises the steps of:

delaying the rising edge of the first clock signal in response to the rising edge compensation signal; and

delaying the falling edge of the first clock signal in response to the falling edge compensation signal.

32. (previously presented) The method of claim 30 wherein the delaying step comprises selectively routing the first clock signal through at least one of a plurality of delay elements to compensate for the phase difference between the first clock signal and the second clock signal.

33. (new) A system for generating clock signals, comprising:

first clocking circuitry operable to generate a first clock signal, the first clocking circuitry operating at a first operating voltage;

second clocking circuitry operable to generate a second clock signal, the second clocking circuitry operating at a second operating voltage;

a phase comparator operable to receive the first and second clock signals and to compare a phase of the first clock signal with a phase of the second clock signal and to generate a compensation signal indicative of a phase difference between the first and second clock signals; and

a delay adjuster configured to receive the compensation signal and operable to delay the first clock signal to compensate for the phase difference between the first and second clock signals.

34. (new) The system of claim 33 wherein the first clock signal drives a first circuit operating at the first operating voltage and the second clock signal drives a second circuit operating at the second operating voltage.

35. (new) The system of claim 9 wherein the common clock signal is provided to the first clocking

circuitry and the second clocking circuitry, wherein the first clocking circuitry is operable to generate the first clock signal based on the common clock signal, and wherein the second clocking circuitry is operable to generate the second clock signal based on the common clock signal.

36. (new) The system of claim 35 wherein the delay adjuster delays the first clock signal by delaying the common clock signal prior to providing the common clock signal to the first clocking circuitry.

37. (new) The system of claim 9 further comprising a level adjuster operable to modify a level of the common clock signal and to provide the modified clock signal to the second clocking circuitry, and wherein the second clocking circuitry is operable to generate the second clock signal based on the modified clock signal.

38. (new) A method for compensating for phase differences between a plurality of clock signals associated with a plurality of signal levels, comprising the steps of:

modifying a signal level of a clock signal to generate a first clock signal having a first signal level that is different than a second signal level of a second clock signal;

comparing a phase of the first clock signal with a phase of the second clock signal to generate at least one compensation signal indicative of a phase difference between the first clock signal and the second clock signal; and

delaying the first clock signal to compensate for the phase difference between the first clock signal and the second clock signal.

39. (new) The method of claim 38 wherein:

the comparing step further comprises the steps of:

comparing a rising edge of the first clock signal with a rising edge of the second clock signal to generate a rising edge compensation signal indicative of a phase difference

between the rising edge of the first clock signal and the rising edge of the second clock signal; and

comparing a falling edge of the first clock signal with a falling edge of the second clock signal to generate a falling edge compensation signal indicative of a phase difference between the falling edge of the first clock signal and the falling edge of the second clock signal;

and the delaying step further comprises the steps of:

delaying the rising edge of the first clock signal in response to the rising edge compensation signal; and

delaying the falling edge of the first clock signal in response to the falling edge compensation signal.

40. (new) The method of claim 38 wherein the delaying step comprises selectively routing the first clock signal through at least one of a plurality of delay elements to compensate for the phase difference between the first clock signal and the second clock signal.